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(71) Applicant : **TEXAS INSTRUMENTS
INCORPORATED**
13500 North Central Expressway
Dallas Texas 75265 (US)
(84) **DE FR IT NL**

(71) Applicant : **TEXAS INSTRUMENTS LIMITED**
Manton Lane
Bedford MK41 7PA (GB)
(84) **GB**

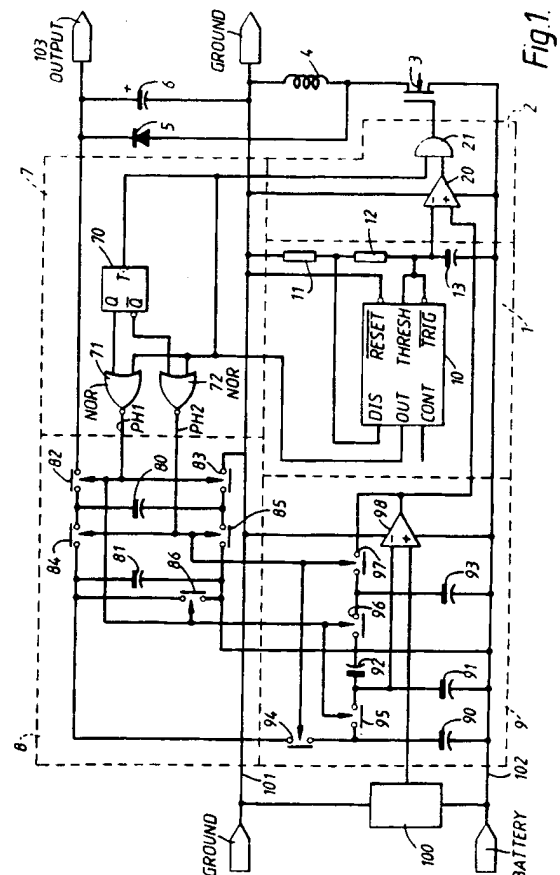
(72) Inventor : **Quarmby, Neil Anthony**
21 Arkwright Road, Milton Ernest,
Bedford, MK44 1SE, (GB)
Inventor : **Eddowes, David William,**
Copperfields, Spring Hill,
Little Staughton, Bedford, MK44 2BE, (GB)

(74) Representative : **Abbott, David John et al**
Abel & Imray Northumberland House 303-306
High Holborn
London, WC1V 7LH (GB)

(54) **A voltage regulator control circuit.**

(57) A voltage regulator control circuit including a capacitor network and a switching network which provides controllable connections among the capacitors of the capacitor network. The switching network is operable to alter the controllable connections in a repeating sequence to provide an output control signal that is a measure of the difference between an input reference voltage applied to the voltage regulator control circuit and a voltage controlled by the voltage regulator control circuit.

The voltage regulator control circuit relies on differential voltage translation and filtering using switched capacitor networks and includes a reference input port for receiving an input reference voltage, a controlled-voltage input port for receiving an output voltage from a voltage regulator to be controlled, a capacitor network, a control signal generator and a switching network for providing controllable connections among capacitors of the capacitor network, the reference input port, the controlled-voltage input port and the control signal generator.



EP 0 547 916 A2

The present invention relates to a voltage regulator control circuit.

A voltage regulator includes a control circuit and output voltage regulating means. In operation, the voltage regulator control circuit drives the output voltage regulating means, and the output voltage regulating means provides the output voltage from the regulator. The voltage regulator control circuit, in operation, compares either the output voltage or a proportion of the output voltage with a constant reference signal and so drives the output voltage regulating means as to hold the output voltage at a level that makes the two voltages being compared substantially equal.

There are several shortcomings of known voltage regulator control circuits, and it is an object of the present invention to reduce at least some of those shortcomings.

The invention provides a voltage regulator control circuit which includes a capacitor network, a control signal generating means, a reference input port for receiving an input reference voltage, a controlled-voltage input port for receiving an output voltage from a voltage regulator which is controlled by the voltage regulator control circuit, and a switching network which provides controllable connections among the capacitors of the capacitor network, the reference input port, the controlled-voltage input port and the control signal generating means, the switching network being operable to alter the controllable connections in a repeating sequence in order to provide, as an output from the control signal generating means, an output control signal which is a measure of the difference between the input reference voltage and the controlled voltage.

More specifically, the invention provides a voltage regulator control circuit including a control signal generating means, a switching network having a plurality of switching elements the states of which are controllable by the control signal generating means, a plurality of capacitors connected together by switching elements of the switching network to form a capacitor network the configuration of which is alterable by alteration of the states of the switching elements, a controlled-voltage input port, for receiving a controlled voltage, connected to the capacitor network by switching elements of the switching network and a reference voltage input port connected to a first input port of comparison means,

the control signal generating means being capable of altering the capacitor network in a repeating sequence of configurations by operating the switching elements of the switching network to provide a proportion of the controlled voltage as a further signal voltage which, in operation, is applied to the comparison means for generating an output signal that is a measure of the difference between an input reference voltage applied to the reference input port and that further signal voltage.

In a first example of the voltage regulator control circuit preferably, the capacitor network includes a node common to all of the capacitors of the network, the switching network includes a switching element connected between an input port of a or the comparison means and the node which is common to all of the capacitors of the network, and, in the operation of the voltage regulator control circuit, a charge which is dependent on the controlled voltage is supplied by the capacitor network to the second input port of the comparison means through the node which is common to the capacitors of the capacitor network.

In the first example of the voltage regulator control circuit, preferably, the comparison means is capable of accumulating the charge which it receives from the capacitor network and, preferably, the capacitor network includes three capacitors connected to the common node.

In a second example of the voltage regulator control circuit, preferably, the capacitor network includes a sampling capacitor, the switching network is operable to connect the sampling capacitor to the controlled-voltage input port in order to provide a measure of the controlled output voltage, and the switching network is further operable to isolate the sampling capacitor from the controlled-voltage input port and to connect the sampling capacitor to a second input port of the or a comparison means.

A voltage regulator control circuit in accordance with the invention, is able to compare the output voltage sample with a constant reference voltage that has any selected datum as its reference. For example, the comparison can be performed with a constant reference voltage derived from a voltage supply of opposite polarity to the output voltage of the regulator and with respect to one of the terminals of the negative input supply and the negative input supply can be present before the voltage regulator operates. The result of the comparison is then always valid since that negative input supply is present before the voltage regulator starts to operate. In known systems, the reference voltage is derived from the output voltage which takes some time to establish itself. The disadvantage in known systems is that the result of the comparison is invalid at start-up.

Another shortcoming of known regulator control circuits arises through their use of a d.c. voltage shifting network for translating a signal obtained from the output voltage to a level at which comparison with a reference voltage is possible; that arrangement gives rise to errors in the measured output voltage. In contrast, the control circuit of the present invention avoids any d.c. shifting. Also, the control circuit of the present invention allows adjustment of the output voltage through the capacitor network.

Preferably, the second example of the voltage regulator control circuit includes a control input capacitor connected to the control input port of the control

signal generating means, for removing a proportion of the stored charge from the sampling capacitor, in order to control the ratio of the controlled output voltage to the voltage obtained from the sampling capacitor. The use of capacitors for providing a proportion of the output voltage contrasts with known regulator control circuits, which employ resistor networks. The difference is significant in the fabrication of the control circuits as monolithic semiconductor integrated circuits.

Preferably, the second example of the voltage regulator control circuit includes at least one intermediate capacitor connected in the switching network which is operable to connect the or each intermediate capacitor to the sampling capacitor and to the second input port of the comparison means. The inclusion of intermediate capacitor storage results in the sampling capacitor sharing its stored energy with the or each intermediate capacitor and effects control the ratio of the output voltage to the voltage obtained from the sampling capacitor.

Preferably, both examples of the voltage regulator control circuit include a switched capacitor filter network connected to control the gain of the control loop. The provision of the switched capacitor filter network ensures that the gain of the control loop is adjustable in order to maintain loop stability.

The use of a switched capacitor filter network contrasts with the known arrangements for regulator control circuit filters, which require high value resistors. Those high value resistors are not readily fabricated as components of a semiconductor integrated circuit, whereas the capacitors and switches of the present arrangement can readily be so fabricated.

Preferably, in both examples of the voltage regulator control circuit, the control signal generating means includes a pulse generator which, in operation, provides drive pulses to the switching network.

The control signal generating means may be connected to operate from an input voltage supply that is of the opposite polarity to the output voltage provided by the voltage regulator which is controlled by the control circuit, the input reference voltage being obtained from means connected to the input voltage supply and the capacitor network being capable of providing a further signal voltage of the correct polarity to the or a comparison means.

The use of capacitors for sampling and scaling the output voltage provides an arrangement which can be readily fabricated as components of a semiconductor integrated circuit. The scaling factor depends on the ratios of the capacitances used, and integrated circuit capacitors with specific capacitance ratios can be made accurately.

A multiple output voltage regulator control circuit, for controlling a voltage regulator which is capable of providing a plurality of controlled output voltages on respective output ports, includes a voltage regulator control circuit as defined above for each controlled

output voltage.

Preferably, each switch element of the switching network is a complementary MOSFET. That arrangement provides a switch comprising complementary components which generate opposing thermal voltages that affect the state of charge of the capacitor network.

Advantageously, the voltage regulator control circuit is fabricated as a monolithic integrated circuit, and, preferably, the multiple output voltage regulator control circuit is fabricated as a monolithic integrated circuit.

Three examples of voltage regulator control circuit in accordance with the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a diagram of a voltage regulator including a first example of a single-output voltage regulator control circuit,

Fig. 2 is a diagram of a voltage regulator including a second example of a single output voltage regulator control circuit and

Fig. 3 is a diagram of a voltage regulator including a multiple-output voltage regulator control circuit.

Referring to Fig. 1 of the accompanying drawings, the voltage regulator includes a control generator 1, a pulse width modulator 2, an insulated gate transistor 3, an inductor 4, a diode 5, a storage capacitor 6, a switch controller 7, a sampling stage 8, a translation stage 9, voltage reference element 100, supply terminals 101 and 102, and output terminals 101 and 103.

The control generator 1 includes a control oscillator 10, resistors 11 and 12, and a timing capacitor 13. The resistors 11 and 12, and the timing capacitor 13, are connected in series between the supply terminals 101 and 102. The capacitor 13 has one of its terminals connected to the supply terminal 102 and the other of its terminals connected to the resistor 12. The resistors 11 and 12, and the capacitor 13, are so connected to the control oscillator 10 as to act as a timing network for the control oscillator 10. The timing oscillator 10 operates to provide a ramp waveform output and a rectangular waveform output. The rectangular waveform is at a first of its two levels during the rising part of the ramp waveform and is at the other of its two levels during the falling part of the ramp waveform.

The pulse width modulator 2 includes a comparator 20 and a two-input AND gate 21. One input terminal of the AND gate 21 is connected to the output of the comparator 20.

The switch controller 7 includes a bistable flip-flop 70, a first two-input NOR gate 71 and a second two-input NOR gate 72. The Q output of the flip-flop 70 is connected to one input of the NOR gate 71 and the Q output of the flip-flop 70 is connected to one input of the NOR gate 72.

The sampling stage 8 includes a first capacitor 80, a second capacitor 81, switch elements 82, 83 and

86 belonging to a first switch network, and switch elements 84 and 85 belonging to a second switch network. The switch elements are complementary MOS-FETs. Each switch element has two transfer terminals and a control terminal, and the voltage applied to the control terminal determines whether the transfer terminals are connected to, or disconnected from, each other. One terminal of the first capacitor 80 is connected to one transfer terminal of the switch element 82 and to a transfer terminal of the switch element 84. The other terminal of the first capacitor 80 is connected to one transfer terminal of the switch element 83 and to a transfer terminal of the switch element 85. One terminal of the second capacitor 81 is connected to the other transfer terminal of the switch element 84, to one transfer terminal of the switch element 86 and to one transfer terminal of the switch element 94. The other terminal of the second capacitor 81 is connected to the other transfer terminal of the switch element 85 and to the other transfer terminal of the switch element 86. The other transfer terminal of the switch element 82 is connected to the terminal 103 and the other transfer terminal of the switch element 83 is connected to the terminal 101.

The translation stage 9 includes a third capacitor 90, a fourth capacitor 91, a fifth capacitor 92, a sixth capacitor 93, switch elements 95 and 96 belonging to the first switch network, switch elements 94 and 97 belonging to the second switch network, and an amplifier 98. One terminal of the third capacitor 90 is connected to the other transfer terminal of the switch element 94 and to a transfer terminal of the switch element 95. The other terminal of the third capacitor 90 is connected to one terminal of the fourth capacitor 91, to one terminal of the sixth capacitor 93 and to the terminal 102. The other terminal of the fourth capacitor 91 is connected to the other transfer port of the switch element 95, to one terminal of the fifth capacitor 92 and to the inverting input terminal of the amplifier 98. The other terminal of the fifth capacitor 92 is connected to one transfer terminal of the switch element 96. The other terminal of the sixth capacitor 93 is connected to the other transfer terminal of the switch element 96 and to one transfer terminal of the switch element 97. The other transfer terminal of the switch element 97 is connected to the output terminal of the amplifier 98.

The supply power input terminals 101 and 102 of the voltage regulator are for receiving d.c. input power, which makes the input terminal 102 negative relative to the input terminals 101, and the switch mode voltage regulator provides an output voltage that makes the terminal 103 positive relative to the terminal 101.

The operation of the voltage regulator is as follows:

The control generator 2 supplies a rectangular waveform output, which is applied to one input termi-

nal of each of the NOR gates 71 and 72 and to the toggle (T) input terminal of the bistable flip-flop 70. The NOR gates 71 and 72 provide alternate non-overlapping pulses PH1 and PH2. The pulse PH1 switches on the switch elements 82, 83, 86, 95 and 96 when it is at its high level and the pulse PH2 switches on the switch elements 84, 85, 94 and 97 when it is at its high level.

When the switch elements 82, 83, 86, 95 and 96 are conductive, the switch elements 84, 85, 94 and 97 are non-conductive, with the result that the capacitor 80 is connected only to the terminals 101 and 103, and is charged to the output voltage of the power supply; at the same time, the switch 86 shunts the capacitor 81 and discharges it. Charge on the capacitor 90 is shared with the capacitors 91, 92 and 93 because the switch elements 95 and 96 are conductive and the resulting common voltage of the capacitors 90 and 91 is applied to the inverting input terminal of the comparator 98.

When the switch elements 84, 85, 94 and 97 are conductive, the switch elements 82, 83, 86, 95 and 96 are non-conductive, with the result that the capacitor 80 is disconnected from the terminals 101 and 102 and is connected in parallel with the capacitors 81 and 90. The datum voltage of the capacitors 80, 81 and 90 is the terminal 102; the original datum voltage of the capacitor 80 was the terminal 101.

The charge accumulated on the capacitor 80 when the switch elements 82 and 83 are conductive amounts to $C_{80} \cdot V_{out}$, where C_{80} is the capacitance of the capacitor 80 and V_{out} is the output voltage, that is, the voltage between the terminals 101 and 103. When the capacitor 80 is connected in parallel with the capacitors 81 and 90, the charge $C_{80} \cdot V_{out}$ is shared among the three capacitors and gives rise to a common voltage V_{com} such that $V_{com} = V_{out} \cdot C_{80} / (C_{80} + C_{81} + C_{90})$. Thus, the voltage V_{out} has been scaled down by a factor $C_{80} / (C_{80} + C_{81} + C_{90})$, which is substantially equal to $C_{80} / (C_{80} + C_{81})$ since C_{80} and C_{90} are much greater than C_{81} , where C_{81} and C_{90} are the capacitances of the capacitors 81 and 90, respectively, and the scaled voltage now has the terminal 102 as its datum. The charge stored on the capacitor 90 is $V_{com} \cdot C_{90}$ and that charge is shared with the capacitors 91, 92 and 93 on the next occasion that the switch elements 95 and 96 are conductive, that being the next occasion on which PH1 is at its high value. The capacitor 93 also shares its charge with the capacitors 90, 91 and 92. The voltage resulting from the sharing of the charges held by the capacitors 90 and 93 is applied to the inverting input terminal of the amplifier 98, which amplifies the difference between the voltage provided by the capacitors 90 and 91 and the voltage applied to the non-inverting input terminal of the amplifier 98 from the voltage reference element 100. That output voltage of the amplifier 98 is sampled and held by the capacitor 93 on the next occasion that

the switch element 97 is conductive and the switch element 96 is non-conductive.

The output voltage from the amplifier 98 represents the difference between a proportion of the output voltage present between the terminals 101 and 103 and the reference voltage from the reference element 100. The output voltage from the amplifier 98 is scaled down by the capacitors 80, 81, 91 and 92 which have substantially greater capacitances than the capacitors 90 and 93. The capacitors 90 and 93, which have relatively low capacitances, act as high value resistors with effective resistances determined by their capacitances and the operating frequency of the switch elements. The capacitors 90, 91, 92 and 93 act as a filter network in which the smaller switched capacitors act, in effect, as resistors having high resistances.

The output voltage from the amplifier 98 is applied to the non-inverting input terminal of the comparator 20 which provides a width-modulated rectangular waveform output voltage, in known manner, for controlling the lengths of the conductive periods of the transistor 3.

The switch elements are operated in two groups. Each group is driven by a single clock pulse and the two clock pulses are complementary and non-overlapping.

The voltage regulator control circuit consists of the components shown within the dotted lines in the accompanying drawing, that is, the control generator 1, the pulse width modulator 2, the switch controller 7, the sampling stage 8, and the translation stage 9.

The voltage regulator control circuit employs differential voltage translation of the output voltage from the voltage regulator, available at the storage capacitor 6, using the switched capacitor network included in the switch controller 7, the sampling stage 8 and the translation stage 9. The switched-capacitor network takes a differential sample of the output voltage by isolating both terminals of the sampling capacitor 80 once the sample has been obtained, scales down the sample by charge sharing among the capacitors 80, 81, 90 and 91, and effects the transfer of the scaled down sample in the transfer of a fixed proportion of the charge originally held by the capacitor 80 to the capacitor 91. The charge transferred to the capacitor 91 is compared with the reference voltage from the reference 100 which is obtained from the input voltage and the difference is amplified by the amplifier 98 and passed to a switched-capacitor filter network (switches 96 and 97, capacitors 92 and 93) which is connected to the amplifier 98. The switched-capacitor filter networks controls the gain of the control loop and is effective to ensure its stability. The switched-capacitor filter network includes only small capacitors and performs functions carried out by very large resistors in conventional active filter networks. The functions of sampling and scaling are performed as a single oper-

ation; the sampling is differential voltage sampling and the scaling is accurate and reproducible when the capacitors are fabricated in a semiconductor integrated circuit because capacitors fabricated by semiconductor fabrication processes can be closely matched in value.

Referring to Fig. 2 of the accompanying drawings, the voltage regulator includes a control generator 201, a pulse width modulator, 202, an insulated gate transistor 203, an inductor 204, a diode 205, a storage capacitor 206, a switch controller 207, a combined sampling and translation stage 208, a voltage reference element 2100, supply terminals 2101 and 2102, and output terminals 2101 and 2103.

The voltage regulator represented by Fig. 2 is substantially the same as that represented by Fig. 1 except that in Fig. 2, the combined sampling and translation stage 208 takes the place of the sampling stage 8 and the translation stage 9 of Fig. 1.

The combined sampling and translation stage 208 includes a first set of switch elements 281, 283, 286, and 288 having their control terminals connected together, and a second set of switch elements 282, 284, 285, and 287 having their control terminal connected together. The control terminals of the first set of switch elements are connected to a first output terminal of the switch controller 207 and that first output terminal provides a first switching pulse PH1. The control terminal of the second set of switch elements are connected to receive a second switching pulse PH2 from the switch controller 207. The pulses PH1 and PH2 do not overlap each other. The combined sampling and translation stage 208 also includes capacitors 289, 290, 291 and 292, and an amplifier 293. One terminal of the capacitor 289 is connected to a transfer terminal of the switch element 283 and to a transfer terminal of the switch element 284. The other terminal of the capacitor 289 is connected to a transfer terminal of the switch element 285, to a transfer terminal of the switch element 286, to one terminal of the capacitor 290 and to one terminal of the capacitor 291. The other terminal of the capacitor 290 is connected to one transfer terminal of the switch element 281 and to one terminal of the switch element 282. The other terminal of the capacitor 291 is connected to one transfer terminal of the switch element 287 and to one transfer terminal of the switch element 288. The capacitor 292 is connected between the output terminal and the inverting input terminal of the amplifier 293, and the inverting input terminal of the amplifier 293 is connected to the other transfer terminal of the switch element 286. The non-inverting input terminal of the amplifier 293 is connected to the reference output terminal of the voltage reference element 2100. The output terminal of the amplifier 293 is connected to the pulse width modulator 202. The other transfer terminal of each of the switch elements 282, 283, 285 and 286 is connected to the reference output

terminal of the voltage reference element 2100, the other transfer terminal of the switch element 281 is connected to the output terminal 2103, the other transfer terminal of the switch element 284 is connected to the terminal 2101, and the other transfer terminal of the switch element 288 is connected to the terminal 2102. The switch elements are complementary MOSFETS.

The combined sampling and translation stage 208 has a first configuration when the switching pulse PH2 is at its high level (at which time the switching pulse PH1 is at its low level). In the first configuration of the combined sampling and translation stage 208, the switch elements 282, 284, 285 and 287 are conductive. The switching pulse PH1 is at its low level and the switch elements 281, 283, 286 and 288 are non-conductive. The capacitor 290 is discharged by the conductive switch elements 282 and 285, and the capacitor 291 is discharged by the conductive switch elements 285 and 287. During that time, the capacitor 289 is connected between the terminal 2101 and the reference output terminal of the voltage reference element 2100 by the conductive switches 284 and 285, and charged to the reference voltage.

The combined sampling and translation stage 208 has a second configuration when the switching pulse PH1 is at its high level (at which time the switching pulse PH2 is at its low level). In the second configuration of the combined sampling and translation stage 208, the switch elements 281, 283, 286 and 288 are conductive and the other switch elements are non-conductive. During that time, the inverting input terminal of the amplifier 293 is connected by way of the switch element 286 to that terminal of the capacitor 289 which is connected to a terminal of the capacitor 290 and to a terminal of the capacitor 291. The capacitor 289 is now connected between the inverting terminal of the amplifier 293 and the reference output terminal of the voltage reference element 2100 (which provides a voltage V_{REF}) by the switch element 283, the capacitor 290 is now connected between the inverting input terminal of the amplifier 293 and the output terminal 2103 (which provides a voltage V_{OUT}) by the switch element 281, and the capacitor 291 is now connected between the inverting input terminal of the amplifier 293 and the terminal 2102 (which provides a voltage V_{BATT}) by the switch element 288. The capacitor 292 is connected directly between the output terminal and the inverting terminal of the amplifier 293; also the non-inverting terminal of the amplifier 293 is connected directly to the reference output terminal of the voltage reference element 2100 and, therefore, is held at V_{REF} .

The capacitors 290 and 291 are held discharged during the pulse PH2 and the capacitor 289 is charged to the voltage V_{REF} . During the pulse PH1, current flows in the capacitor network and the average current I_{AV} , due to the capacitors 289, 290 and 291, at the in-

verting terminal of the amplifier 293 may be expressed as:

$$I_{av} = 1/T(V_1 \times C_{289} - V_2 \times C_{291} + V_3 \times C_{290})$$

where T is the duration of the pulse PH1, V_1 , V_2 and V_3 are, respectively, the output voltage, the ground voltage and the battery voltage relative to the reference voltage V_{REF} and C_{289} , C_{290} and C_{291} are the respective capacitances of the capacitors 289, 290 and 291.

In Fig. 2, the capacitances C_{289} and C_{291} are equal to each other and the expression for I_{AV} becomes

$$I_{av} = 1/T[(V_1 - V_2) \cdot C_{289} + V_3 \times C_{290}]$$

which may be expressed as:

$$I_{av} \cdot T = (V_{out} \times C_{289} - V_{ref} \times C_{290})$$

where V_{OUT} is the output voltage with respect to ground and V_{REF} is the reference voltage with respect to the battery voltage.

The charge $I_{AV} \cdot T$ may be expected to provide an output voltage V_{INT} from the amplifier 293 and the capacitor 292 which may be expressed as follows:

$$V_{cont} = I_{av} \cdot T / C_{292} = V_{out} \times C_{289} / C_{292} - V_{ref} \times C_{290} / C_{292}$$

where C_{292} is the value of the capacitor 292.

The voltage V_{CONT} represents the difference between the proportion C_{289}/C_{292} of the output voltage V_{OUT} and the proportion C_{290}/C_{292} of the reference voltage V_{REF} .

The expression for V_{CONT} becomes

$$V_{cont} = V_{out} \times C_{289}/C_{292} - V_{ref} \text{ when } C_{290} = C_{292}.$$

The output voltage from the amplifier 293 is applied to the ramp generator 201 and controls the output voltage V_{OUT} .

A switched-capacitor filter network can be included between the amplifier 293 and the pulse width modulator stage 202 as a means of controlling the loop gain of the system.

Referring to Fig. 3 of the accompanying drawings, the voltage regulator includes all of the second form of voltage regulator control circuit and, also, an additional sampling and translation stage 308, and an additional pulse width modulator 302. The voltage regulator includes, also, the output components of the voltage regulator shown in Fig. 2, and an additional set of output components 303, 304, 305 and 306, which provide a second output voltage on a second output terminal 3103.

The additional sampling and translation stage 308 receives the switching pulses PH1 and PH2 provided by the switch controller 207 and is connected to the reference voltage terminal of the reference element 2100. The additional pulse width modulator 302 receives the ramp output and drive pulse from the control generator 201 and supplies width-modulated drive pulses to the transistor 303. The values of the capacitors of the additional sampling and translation stage 308 differ from the values of the respective capacitors in the sampling and translation stage 208, with the result that the second output voltage avail-

able at the terminal 3103 differs from the output voltage available at the terminal 2103. Apart from the differences in the values of their capacitors, the sampling and translation stages 208 and 308 are identical. The pulse width modulators 202 and 302 are also identical.

The number of output terminals can be increased above the two shown in Fig. 3 by the addition of further sampling and translation stages and pulse width modulators, connected to further output components and to the sampling and translation stage 208, the control generator 201, and to the voltage reference element 2100 as shown in Fig. 3. The output voltages need not all be different since it may be desirable, in some circumstances, to have the same voltage available at more than one output terminal, for example, where a single output cannot supply the current required or it is desirable to reduce cross-talk between parts of a system requiring only one supply voltage.

The third voltage regulator control circuit consists of the components 201, 202, 207, 208, 2100, 302 and 308.

A plurality of output voltages are obtainable from the voltage regulator using the third voltage regulator control circuit, shown in Fig. 3, using a single voltage reference element 2100. That arrangement has the desirable feature, in integrated circuit forms of the voltage regulator control circuit, there is only one reference element to be trimmed.

The voltage regulator control circuits described above all have the desirable feature that, in integrated circuit form, the switch elements and capacitors require relatively small amounts of semiconductor material.

Claims

1. A voltage regulator control circuit which includes a capacitor network, a control signal generating means, a reference input port for receiving an input reference voltage, a controlled-voltage input port for receiving an output voltage from a voltage regulator which is controlled by the voltage regulator control circuit, and a switching network which provides controllable connections among the capacitors of the capacitor network, the reference input port, the controlled-voltage input port and the control signal generating means, the switching network being operable to alter the controllable connections in a repeating sequence in order to provide, as an output from the control signal generating means, an output control signal which is a measure of the difference between the input reference voltage and the controlled voltage.
2. A voltage regulator control circuit including a con-

trol signal generating means, a switching network having a plurality of switching elements the states of which are controllable by the control signal generating means, a plurality of capacitors connected together by switching elements of the switching network to form a capacitor network the configuration of which is alterable by alteration of the states of the switching elements a controlled-voltage input port, for receiving a controlled voltage, connected to the capacitor network by switching elements of the switching network and a reference voltage input port connected to a first input port of comparison means,

the control signal generating means being capable of altering the capacitor network in a repeating sequence of configurations by operating the switching elements of the switching network to provide a proportion of the controlled voltage as a further signal voltage which, in operation, is applied to the comparison means for generating an output signal that is a measure of the difference between an input reference voltage applied to the reference input port and that further signal voltage.

3. A voltage regulator control circuit as claimed in claim 1 or claim 2, wherein the capacitor network includes a node common to all of the capacitors of the network, the switching network includes a switching element connected between a second input port of a or the comparison means and the node which is common to all of the capacitors of the network, and, in the operation of the voltage regulator control circuit, a charge which is dependent on the controlled voltage is supplied by the capacitor network to the second input port of the comparison means through the node which is common to the capacitors of the capacitor network.
4. A voltage regulator control circuit as claimed in claim 3, wherein the comparison means is capable of accumulating the charge which it receives from the capacitor network.
5. A voltage regulator control circuit as claimed in any one of claims 1 to 4, wherein the capacitor network includes three capacitors connected to the common node.
6. A voltage regulator control circuit as claimed in claim 1 or claim 2, wherein the capacitor network includes a sampling capacitor, the switching network is operable to connect the sampling capacitor to the controlled-voltage input port in order to provide in the sampling capacitor a measure of the controlled output voltage, and the switching network is further operable to isolate the sampling

capacitor from the controlled-voltage input port and to connect the sampling capacitor to a second input port of a or the comparison means.

15. A voltage regulator including a voltage regulator control circuit as claimed in any one of claims 1 to 14.

7. A voltage regulator control circuit as claimed in claim 6, which includes a control input capacitor connected to the control input port of the control signal generating means, for removing a proportion of the stored charge from the sampling capacitor in order to control the ratio of the controlled output voltage to the voltage obtained from the sampling capacitor. 5
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8. A voltage regulator control circuit as claimed in claim 6 or 7, which includes at least one intermediate capacitor connected in the switching network which is operable to connect the or each intermediate capacitor to the sampling capacitor and to the second input port of the comparison means, for removing a proportion of the stored charge from the sampling capacitor. 15
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9. A voltage regulator control circuit as claimed in any one of claims 1 to 8, further including a switched capacitor filter network connected to control the gain of the control loop. 25
10. A voltage regulator control circuit as claimed in any one of claims 1 to 9, including a pulse width modulated output means driven by the control signal generating means which includes a pulse generator which, in operation, provides drive pulses to the switching network. 30
11. A voltage regulator control circuit as claimed in any one of claims 1 to 10, wherein the control signal generating means is connected to operate from an input voltage supply which is of the opposite polarity to the output voltage provided by the voltage regulator, the input reference voltage being obtained from means connected to the input voltage supply and the capacitor network being capable of providing a further signal voltage of the correct polarity to a or the comparison means. 35
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12. A multiple output voltage regulator control circuit, including a voltage regulator control circuit as claimed in any one of claims 1 to 11 for each of a plurality of controlled output voltage ports. 50
13. A voltage regulator control circuit as claimed in any one of claims 1 to 11, fabricated as a monolithic integrated circuit. 55
14. A multiple output voltage regulator control circuit as claimed in claim 12, fabricated as a monolithic integrated circuit. 55

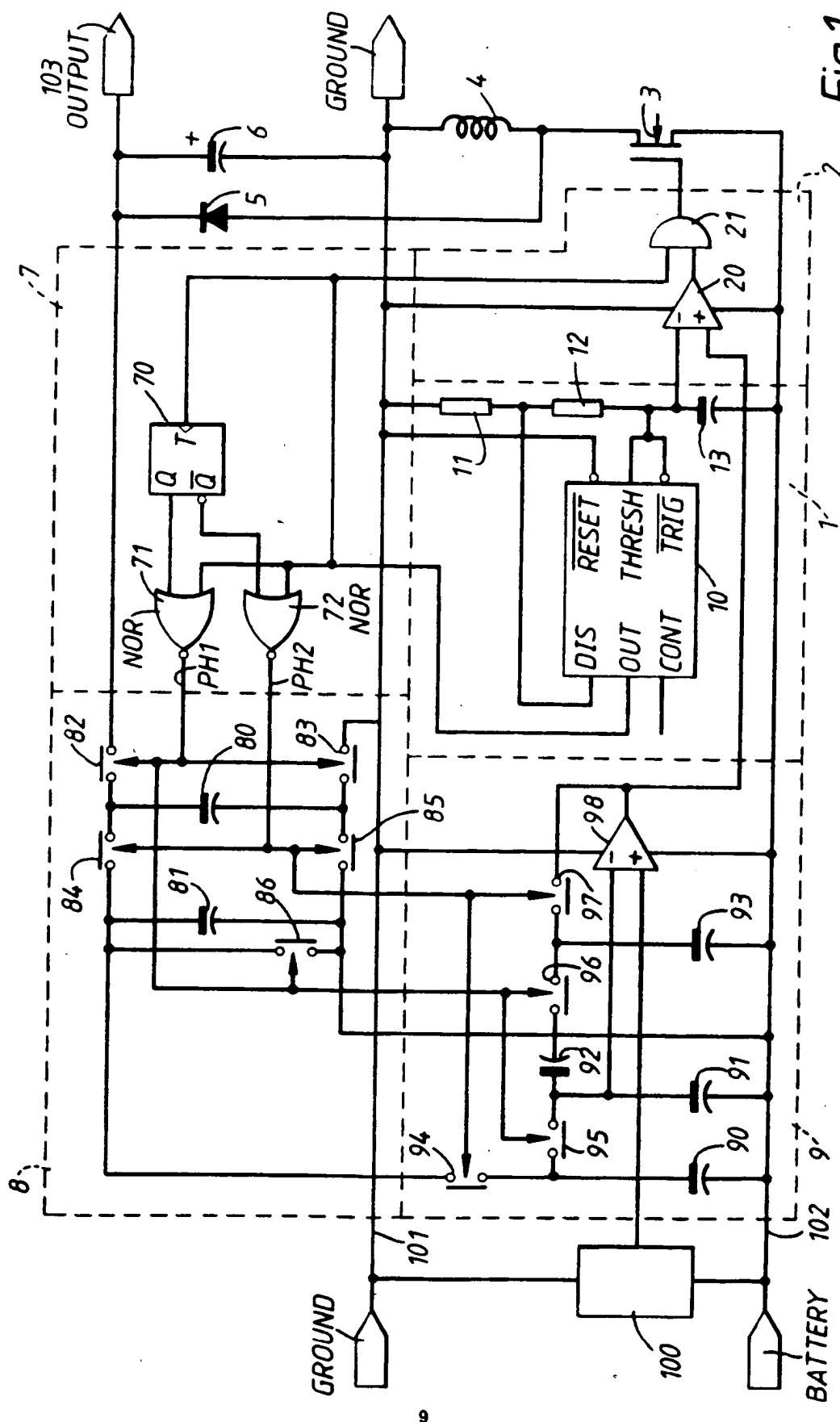


Fig.1.

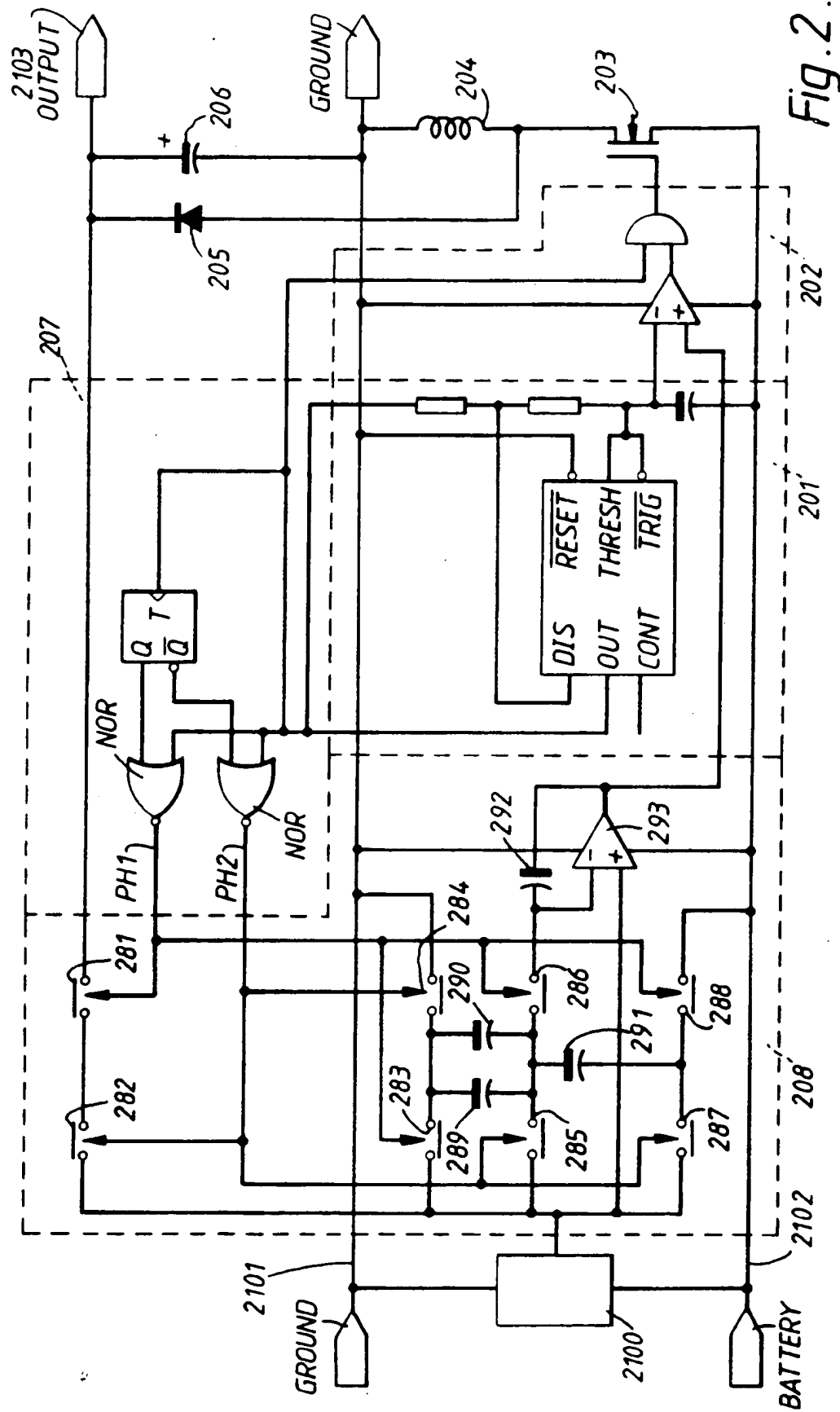


Fig. 2.

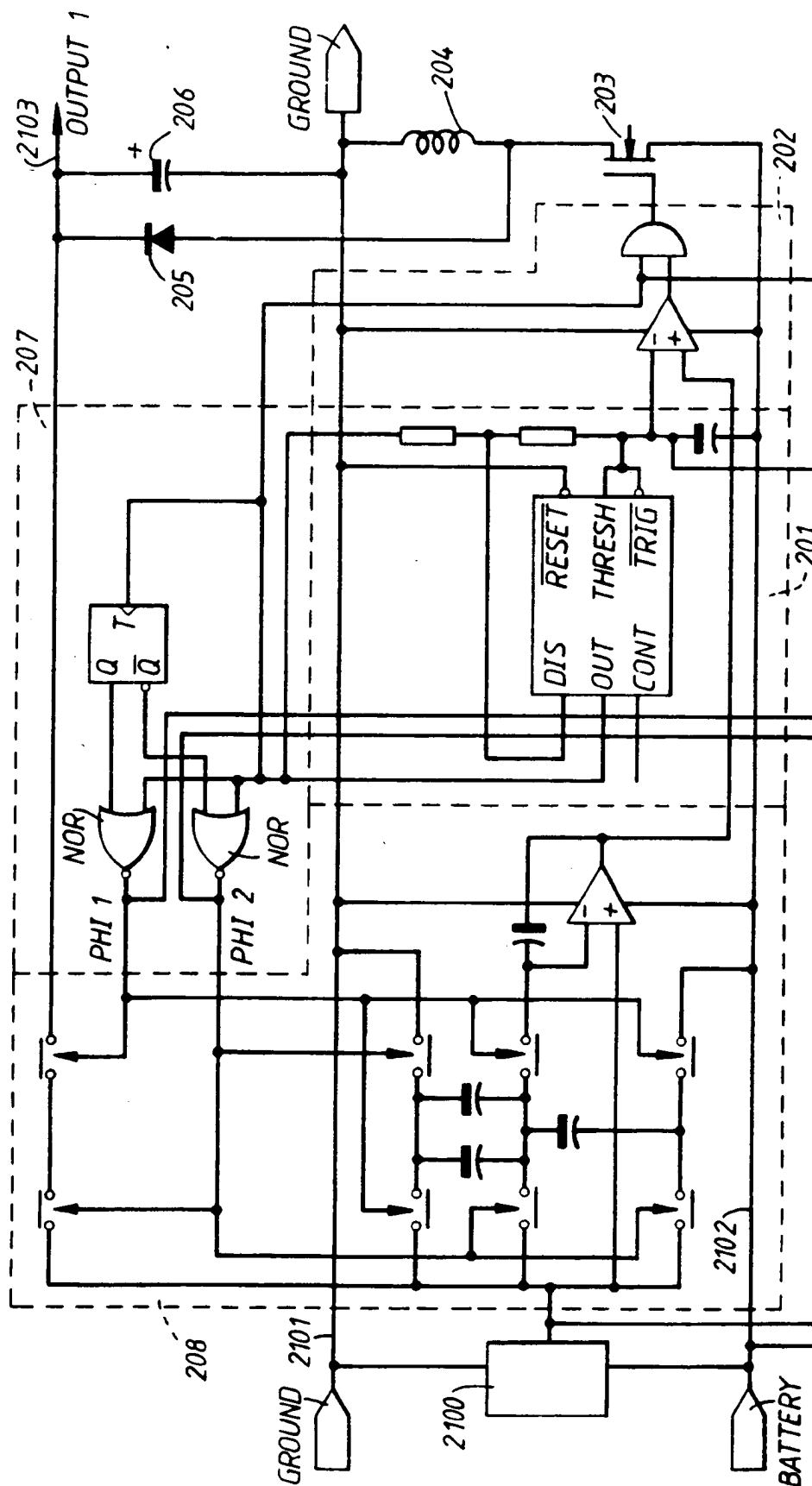


Fig. 3.

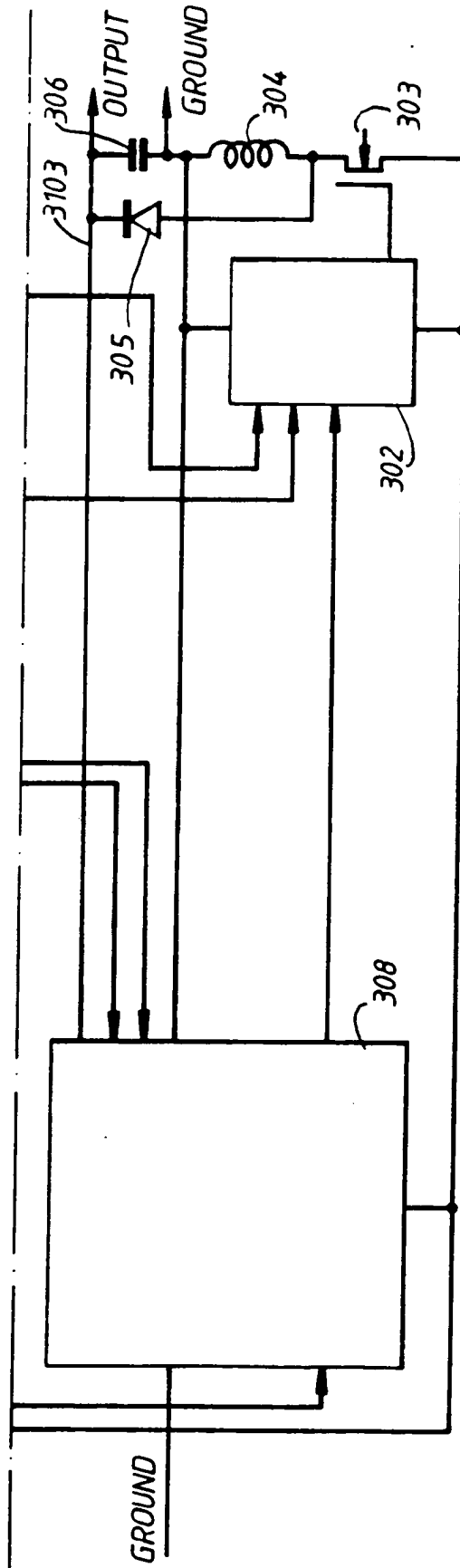


Fig. 3. cont